30V P-Ch Power MOSFET

V_{DS}		-30	V
$R_{DS(on),typ}$	V_{GS}=10V	42	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	66	mΩ
$I_{D\ (Sillicon\ Limited)}$		-5	A

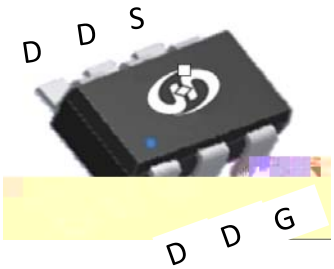
Feature

High Speed Power Switching, Logic Level
Enhanced Avalanche Ruggedness
Lead Free, Halogen Free

A

Gate

TSOP-6



Src

Part Number	Package	Marking
HTO500P03	TSOP-6	23

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	-5	A
		T_C=70	-4.2	
Drain to Source Voltage	V_{DS}	-	-30	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	-20	A
Power Dissipation	P_D	T_C=25	1	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	100	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-1.0	-1.5	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-24V, T_j=25	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-20V, T_j=125	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-5A	-	42	50	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	66	85	
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-5A	-	9	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz	-	820	-	pF
Output Capacitance	C_{oss}		-	122	-	
Reverse Transfer Capacitance	C_{rss}		-	97	-	
Total Gate Charge	Q_g(10V)	V_{DD}=-15V, I_D=-5A, V_{GS}=-10V	-	9.0	-	nC
Gate to Source Charge	Q_{gs}		-	2.2	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	2.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=-15V, I_D=-1A, V_{GS}=-10V, R_G=6Ω,	-	12	-	ns
Rise time	t_r		-	16	-	
Turn off Delay Time	$t_{d(off)}$		-	34	-	
Fall Time	t_f		-	20	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-3A	-		-1.2	V

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

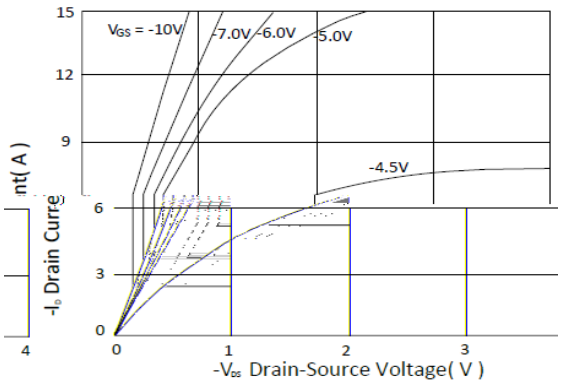
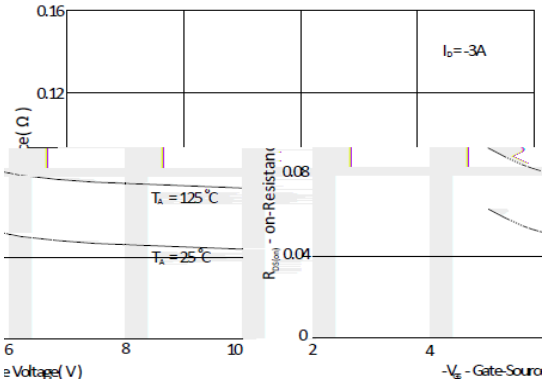

	

Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature

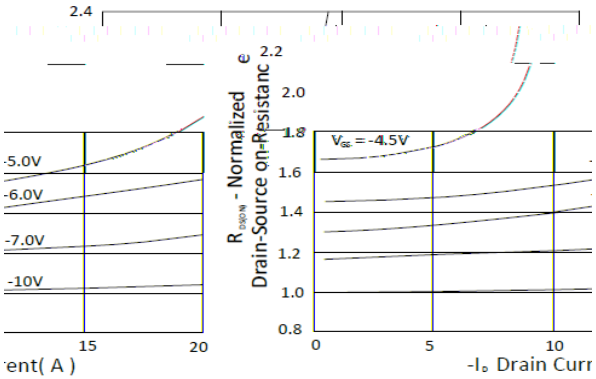
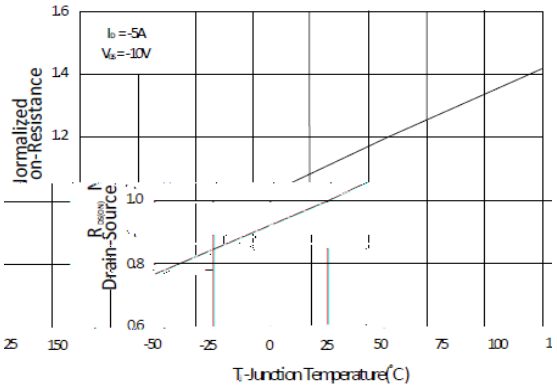

	

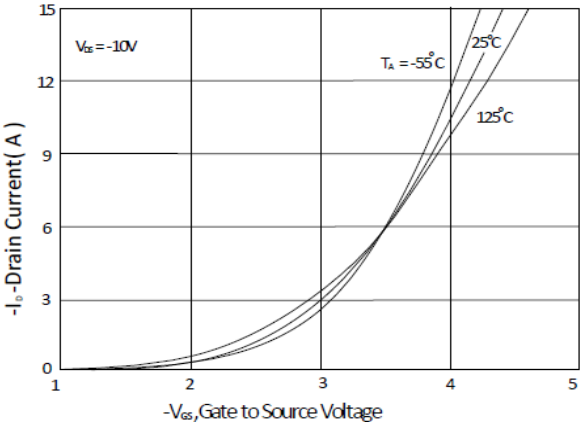
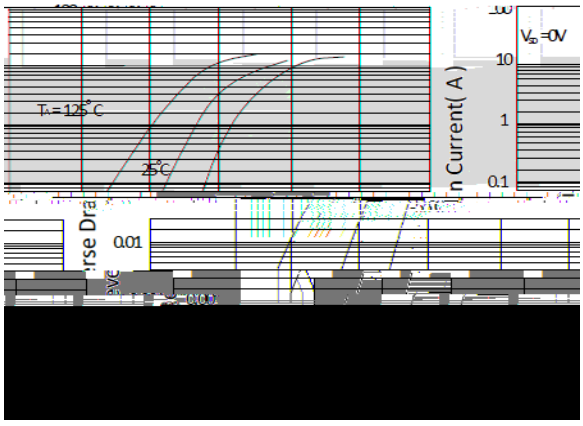
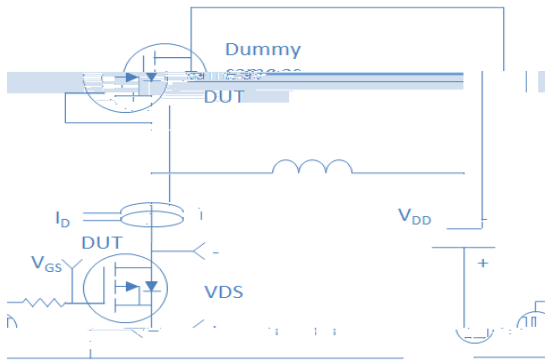
Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage
	

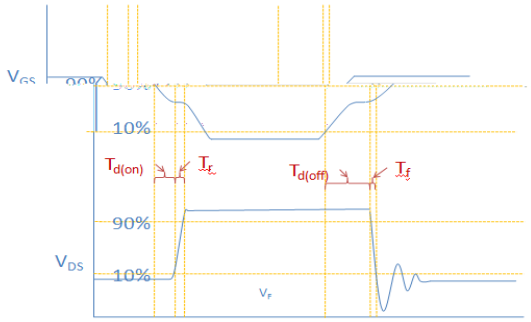
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area	Figure 10. Single Pulse Maximum Power Dissipation

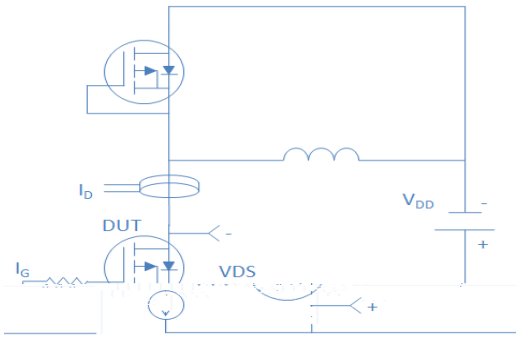
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

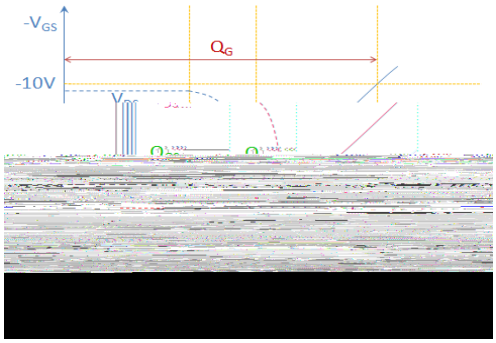
Inductive switching Test



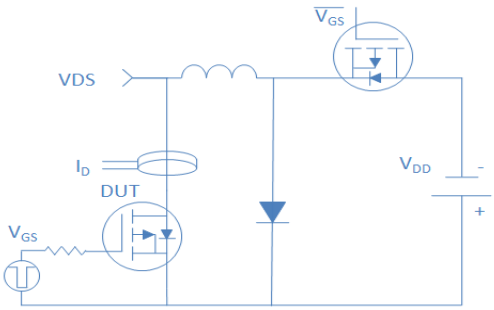


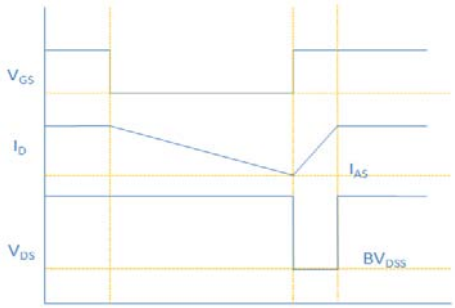
Gate Charge Test



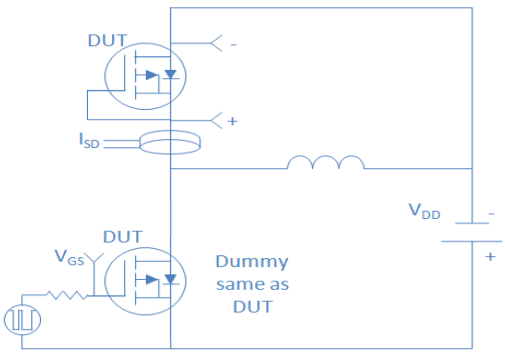


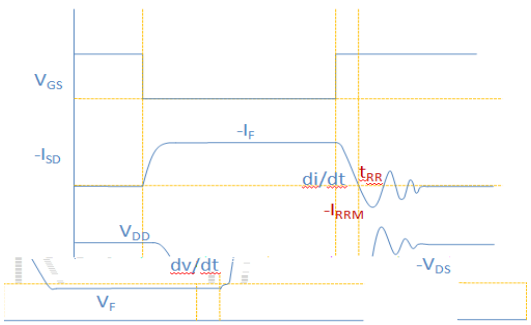
Uclamped Inductive Switching (UIS) Test





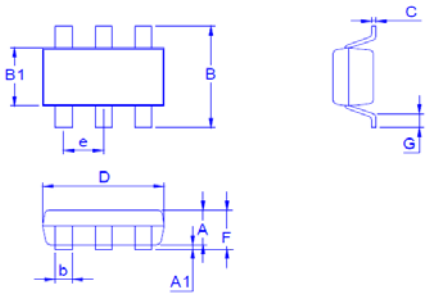
Diode Recovery Test





Package Outline

TSOP-6, 6leads



Dimension in mm

Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.90	0.85	0	2.53	1.50	0.30	3.03	2.60		0.35
Typ.		0.95		2.80	1.60	0.40		2.90	0.95	
Max.	1.05	1.05	0.15	3.10	1.70	0.50	3.20	3.10		1.48